IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

In re Application of: Serial No. 10/525,139 Application of: Emmanuel Ardichvili and Christophe Floret Filed: February 16, 2005 For: DELAY LINE FOR MULTIPLE PROPAGATION PATHS RECEPTION	Confirmation No.: 1770 Art Unit: 2611 Examiner: Aristocratis Fotakis Customer No.: **25235**

Mail Stop Appeal Brief - Patents
Commissioner for Patents
P.O. Box 1450
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APPELLANT'S BRIEF UNDER 37 CFR § 41.37

I. Real Party in Interest

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II. Related Appeals and Interferences

No other appeals or interferences are currently known to Appellant that will directly affect, be directly affected by, or have a bearing on the decision to be rendered by the Board of Patent Appeals and Interferences in the present appeal.

III. Status of Claims

Claims 1-14 are pending in the application, with no claims being cancelled. No claims have been allowed, and all pending claims stand rejected.

Claims 1-10, 12 and 13 were rejected under 35 USC § 103(a) as being unpatentable over U.S Patent Application Publication No. 2002/0037027 by Medlock ("Medlock") in view of Appellant Admitted Prior Art (AAPA).

Claim 11 was rejected over Medlock and AAPA, in further view of U.S. Patent 6,788,731 by Kim ("Kim").

Claim 14 was rejected over Medlock in view AAPA and in further view of Kim.

The rejection of claims 1, 6 and 12-14 under 35 U.S.C. § 103(a) is the subject of this appeal.

IV. Status of Amendments

Appellant believes that all claim amendments prior to the Response to Final Office Action of November 12, 2009 have been entered. In the Final Office Action dated November 12, 2009 the Examiner objected to claim 1 for minor informalities. Specifically, the Examiner objected to the lack of commas encasing the phrase "after a last sample of the series of samples is received." In the Response filed January 12, 2009 the commas were added meeting the Examiner's recommendation. However, the Advisory Action January 28, 2010 fails to indicate the status of the proposed amendment. For the sake of clarity, the amendments proposed in the Response to Final Office action of January 12, 2010 are again submitted as found in the claims listed in the Appendix.

Claims 1-14, including any proposed and entered claim amendments, are provided in the attached Claims Appendix.

V. Summary of Claimed Subject Matter

The following concise explanation of the subject matter defined in each independent claim involved in this Appeal (claims 1, 12, 13 and 14) refers to the specification as originally filed on February 16, 2005 (WO2004/019510) by page and line numbers, and to the drawings by reference characters.

Claim 1 states:

> A receiver for receiving an input signal comprising a series of samples, said receiver comprising one delay line, characterized in that the delay line is configured to delay said input signal by a series of delays and is divided into a series of delay sub-lines, each sub-line being used to write only a single sample from the series of samples of said input signal, each of the delay sub-lines including a separate memory area to receive the single sample from the series of samples, and further comprising control means configured to generate, after a last sample of the series of samples is received, read and write addresses of the samples in the delay sub-lines from the series of samples of the input signal, so that a read address is equal to a difference between the write address of the single sample in a delay sub-line of the input signal and a delay expressed as a number of sampling periods from the series of delays, and wherein the delay sub-lines are directly joined to a plurality of multiplexers for providing early, in-time, and late outputs, and thereafter to a plurality of demodulators for parallel recombination in a coherent manner to find common information according to the delay.

The claims of the present invention describe, in varying language, a receiver configured for receiving an input signal comprising a series of samples. The receiver further comprises a delay line, as well as a method of delaying an input signal, which permit to process multiple paths in a high-performance way without utilizing costly systems in terms of energy consumption and silicon surface. The features of the present invention are shown in Figures 1 – 3 along with pertinent portions of the specification.

As described on page 4, beginning on line 14 and as shown in Figures 1 and 2, a receiver RECEP is utilized in the domain of mobile telephony and notably integrated in a portable telephone. The receiver RECEP operates according to the UMTS standard. At the receiver end RECEP, each received signal is demodulated in the baseband and then sampled by an analog/digital converter. Pg. 4 lines 23-25.

Indeed, the discussion of Figure 2 beginning on page 5, line 8, describes a receiver RECEP with a delay line D_LINE that delays the input signal INPUT. Moreover, the delay line D_LINE is according to one embodiment, divided into a series of delay sub-lines ZONE, that number being the same number as the number of samples in a series of samples. Each delay sub-line ZONE writes a sample from the

series of samples IN_TIME, EARLY, LATE, VOID of an input signal INPUT. Pg 6, lines 12-15.

A memory area is associated with each of the series of the delay sub-lines ZONE. Pg. 6, lines 16-18. Moreover, the illustrated example on the bottom of page 6 (lines 30-35) describes a series of samples S arriving at the delay line D_LINE. The 4 samples S1, S2, S3, S4, are written in 4 write registers REG0, REG1, REG2 and REG3 as is shown in Fig. 4.

A control means RD_ADD_GEN generates read addresses so that they are equal to a difference between a write address of a sample in the delay sub-lines ZONE of the input signal and the delays τ applied to the input signal. Pg. 7, lines 31-34. Such a means is described in the example mentioned above at the bottom of page 6, top of page 7. There the specification states, "when the last sample S4 has been received, the write address generator WR_ADD_GEN generates 4 write addresses ADD, one for each of the delay sub-lines ZONE0 to ZONE3, and the 4 samples S1 to S4 are written (WR2) in each of the delay sub-lines ZONE0 to ZONE3." Page 7, lines 5-9.

The specification further describes that the read addresses of the samples in the delay sub-lines are generated so that each read address is equal to a difference between a write address of a sample in the delay sub-line of the input signal and a delay expressed as a number of sampling periods. Pg. 2, lines 27-30.

An example of such an address generation is seen on page 16, lines 8-11 and lines 23-29. Thus, for each reference sample received, one has a read address equal to its write address minus the part of the delay associated with the corresponding path divided by 2, the delay of a path being known of the receiver.

The remainder of claim 1 describes the delay sub-lines being directly joined to a plurality of multiplexers and thereafter a plurality of demodulators for parallel recombination in a coherent manner. Page 19, lines 11-16, describes the use of both multiplexers with the application of a demodulator described in lines 28-30 of the same page. Specifically, the specification states, "Said demodulator DEMOD combines each sample IN_TIME with a code relating to the associated path FING.

Subsequently, all the reference samples IN_TIME are summed up to find back the common information ." Pg. 19, line 28-Pg. 20, line 3. Having identified and separated all the various samples received of the received input signals they are then recombined in a coherent manner to recover the common information. Pg. 11, lines 11-13.

Claim 12 states:

> A delay line for delaying an input signal, said input signal comprising a series of samples, characterized in that the delay line is configured to delay said input signal by a series of delays and is divided into a series of delay sub-lines each sub-line being used to write only a single sample from the series of samples of said input signal, each of the delay sub-lines including a separate memory area to receive the single sample from the series of samples, and in that the delay line comprises control means configured to generate, after a last sample of the series of samples is received, read and write addresses of the samples in the delay sub-lines from the series of samples of the input signal, so that a read address is equal to a difference between the write address of the single sample in a delay sub-line of the input signal and a delay expressed as a number of sampling periods of the series of delays, and wherein the delay sub-lines are directly joined to a plurality of multiplexers for providing early, in-time, and late outputs and therefore to a plurality of demodulators for parallel recombination in a coherent manner to find common information according to the delay.

Claim 12 is directed to the delay line for delaying an input signal received by a receiver. As in claim 1, the delay line D_LINE delays the input signal INPUT received by the receiver. See Figure 2 , Pg. 5, line 8-12. The delay line D_LINE is divided into a series of delay sub-lines ZONE, that number being the same number as the number of samples in a series of samples received by the receiver. Each delay sub-line ZONE writes a sample from the series of samples IN_TIME, EARLY, LATE, VOID of an input signal INPUT. Pg 6, lines 12-15.

A memory area is associated with each of the series of the delay sub-lines ZONE. Pg. 6, lines 16-18. As illustrated in the example on the bottom of page 6 (lines 30-35), a series of samples S arriving at the delay line D_LINE are divided into sub-lines which are then associated with a separate memory, each memory receiving a separate sample. The example describes 4 samples S1, S2, S3, S4, written to 4 write registers REG0, REG1, REG2 and REG3. See also Fig. 4.

A control means RD_ADD_GEN generates read addresses, after the last sample has been received, so that they are equal to a difference between a write address of a sample in the delay sub-lines ZONE of the input signal and the delays τ as applied to the input signal. Pg. 7, lines 28-34. Such a means is described in the example mentioned above at the bottom of page 6, top of page 7. There the specification states, "when the last sample S4 has been received, the write address generator WR_ADD_GEN generates 4 write addresses ADD, one for each of the delay sub-lines ZONE0 to ZONE3, and the 4 samples S1 to S4 are written (WR2) in each of the delay sub-lines ZONE0 to ZONE3." Page 7, lines 5-9.

The specification further describes that the read addresses of the samples in the delay sub-lines are generated so that each read address is equal to a difference between a write address of a sample in the delay sub-line of the input signal and a delay expressed as a number of sampling periods. Pg. 2, lines 27-30, page 7, lines 28-30.

An example of such an address generation is seen on page 16, lines 8-11 and lines 23-29. Thus, for each reference sample received, one has a read address equal to its write address minus the part of the delay associated with the corresponding path divided by 2, the delay of a path being known of the receiver.

The delay sub-lines are thereafter directly joined to a plurality of multiplexers and thereafter a plurality of demodulators for parallel recombination in a coherent manner. Page 19, lines 11-16, describes the use of both multiplexers with the application of a demodulator described in lines 28-30 of the same page. Specifically, the specification states, "Said demodulator DEMOD combines each sample IN_TIME with a code relating to the associated path FING. Subsequently, all the reference samples IN_TIME are summed up to find back the common information ." Pg. 19, line 28-Pg. 20, line 3. Having identified and separated all the various samples received of the received input signals, they are then recombined in a coherent manner to recover the common information. Pg. 11, lines 11-13.

Claim 13 is directed to the method for delaying an input signal by using a delay line. The method begins with the receipt of an input signal by means of a delay

line. The delay line is thereafter divided into a series of delay sub-lines and configured so that each sub-line receives a single sample from the series of samples found in the input signal. Each delay sub-line is associated with a separate memory location that is configured to receive a single sample. The input signal conveyed via the delay sub-lines is delayed by a series of delays.

After the single sample in the series of samples is received, the method continues by generating read and write addresses of the samples in the delay sub-lines so that the read address is equal to the difference between the write address of the single sample in the delay line and a delay expressed as the number of sampling periods of the series of delays.

From that point the sub-lines are directly joined to a plurality of multiplexers and then to a plurality of demodulators to arrive in a coherent manner common information.

Claim 13 states:

> A method of delaying an input signal by means of a delay line, said input signal comprising a series of samples, characterized in that it comprises the steps of:
>
> dividing the delay line into a series of delay sub-lines each sub-line configured to receive a single sample from the series of samples of the input signal, each of the delay sub-lines including a separate memory area to receive the single sample, said delay line being configured to delay said input signal by a series of delays,
>
> generating, after the single sample of the series of samples is received, read and write addresses of the samples in the delay sub-lines from the series of samples of the input signal, so that a read address is equal to a difference between the write address of the single sample in a delay sub-line of the input signal and a delay expressed as a number of sampling periods of the series of delays, and
>
> directly joining the delay sub-lines to a plurality of multiplexers for providing early, in-time, and late outputs, and thereafter to a plurality of demodulators for parallel recombination in a coherent manner to find common information according to the delay.

The method begins with an input signal which is presumably received by a receiver of some sort but is associated with a delay line D_LINE that delays the input signal INPUT. Pg. 5, line 8. The delay line D_LINE is divided into a series of delay

sub-lines ZONE, that number being the same number as the number of samples in a series of samples. Thus, each delay sub-line ZONE receives a single sample from the series of samples IN_TIME, EARLY, LATE, VOID of an input signal INPUT. Pg 6, lines 12-15.

A single memory area is associated with each delay sub-line ZONE. Pg. 6, lines 16-18. Moreover, the illustrated example on the bottom of page 6 (lines 30-35) describe a series of samples S arriving at the delay line D_LINE. The 4 samples S1, S2, S3, S4, are written in 4 write registers REG0, REG1, REG2 and REG3 as is shown in Fig. 4.

The method continues by generating read addresses so that they are equal to a difference between a write address of the single sample in a delay sub-line ZONE of the input signal and the delay τ applied to the input signal. Pg. 7, lines 31-34. Such a means is described in the example mentioned above at the bottom of page 6, top of page 7.

The specification further describes that the read addresses of the samples in the delay sub-lines are generated so that each read address is equal to a difference between a write address of a sample in the delay sub-line of the input signal and a delay expressed as a number of sampling periods of the series of delays. Pg. 2, lines 27-30.

An example of an address generation is seen on page 16, lines 8-11 and lines 23-29. Thus, for each reference sample received, a read address is generated equal to its write address minus the part of the delay associated with the corresponding path divided by 2, the delay of a path being known of the receiver.

Finally claim 13 describes the joining of the delay sub-lines to a plurality of multiplexers providing early, in-time and late outputs and thereafter a plurality of demodulators for parallel recombination in a coherent manner. Page 19, lines 11-16 describes the use of both multiplexers with the application of a demodulator described in lines 28-30 of the same page. Specifically the specification states, "Said demodulator DEMOD combines each sample IN_TIME with a code relating to the

associated path FING. Subsequently, all the reference samples IN_TIME are summed up to find back the common information ." Pg. 19, line 28-Pg. 20, line 3. Having identified and separated all the various samples received of the received input signals they are then recombined in a coherent manner to recover the common information. Pg. 11, lines 11-13.

As with claim 1, claim 14 describes a receiver for receiving an input signal having a series of samples. Claim 14 also includes added detail with respect to the recombination of the delay lines to achieve coherent information.

Claim 14 states:

> A receiver for receiving an input signal comprising a series of samples, said receiver comprising one delay line, characterized in that the delay line is configured to delay said input signal by a series of delays and is divided into a series of delay sub-lines each sub-line being used to write only a single sample from the series of samples of said input signal, each of the delay sub-lines including a separate memory area to receive the single sample from the series of samples, and further comprises control means configured to generate, after the single sample of the series of samples is received, read and write addresses of the samples in the delay sub-lines from the series of samples of the input signal, so that a read address is equal to a difference between the write address of the single sample in a delay sub-line of the input signal and a delay expressed as a number of sampling periods from the series of delays, wherein the delay line comprises various series of delay sub-lines joined directly to a plurality of multiplexers for parallel recombination in a coherent manner, two series of samples are read in parallel, and the separate memory areas are regrouped into a first and a second group, the first group regrouping a current series of current areas and a next series of areas which can each correspond to the first series of delay sub-lines and the second group regrouping the current series of areas and the next series of areas which can each correspond to the second series of the delay sub-lines, so that the separate memory areas for a series of samples read are identical for each equal position factor value.

As with claim 1, claim 14 describes a receiver RECEP such as those utilized in the domain of mobile telephony and notably integrated in a portable telephone that operates according to the UMTS standard. At the receiver end RECEP, each received signal is demodulated in the baseband and then sampled by an analog/digital converter. Pg. 4, line 14, lines 23-25, see also Figures 1, 2. Figure 2, and the text beginning on page 5, line 8, describe a receiver RECEP with a delay line D_LINE

that delays the input signal INPUT by series of delays. Moreover, the delay line D_LINE is divided into a series of delay sub-lines ZONE, that number being the same number as the number of samples in a series of samples thus each sub-line is associated with a single sample. Accordingly, each delay sub-line ZONE writes a sample from the series of samples IN_TIME, EARLY, LATE, VOID of an input signal INPUT. Pg 6, lines 12-15.

A separate memory area is associated with each of the series of the delay sub-lines ZONE meaning each of the sub-lines receives a single sample from the series of samples. Pg. 6, lines 16-18. The illustrated example on the bottom of page 6 (lines 30-35) describe a series of samples S arriving at the delay line D_LINE. The 4 samples S1, S2, S3, S4, are written in 4 write registers REG0, REG1, REG2 and REG3 as is shown in Fig. 4.

A control means RD_ADD_GEN generates read addresses so that they are equal to a difference between a write address of a sample in the delay sub-line ZONE of the input signal and the delays τ applied to the input signal were τ is expressed as the number of sampling periods from the series of delays. Pg. 7, lines 31-34. Such a means is also described in the example mentioned above at the bottom of page 6, top of page 7. There the specification states, "when the last sample S4 has been received, the write address generator WR_ADD_GEN generates 4 write addresses ADD, one for each of the delay sub-lines ZONE0 to ZONE3, and the 4 samples S1 to S4 are written (WR2) in each of the delay sub-lines ZONE0 to ZONE3." Page 7, lines 5-9.

Again, the specification describes that the read addresses of the samples in the delay sub-lines are generated so that each read address is equal to a difference between a write address of a sample in the delay sub-line of the input signal and a delay expressed as a number of sampling periods. Pg. 2, lines 27-30.

The example described on page 16, lines 8-11 and lines 23-29, illustrates the address generation process. For each reference sample received, a read address is generated equal to its write address minus the part of the delay associated with the corresponding path, a delay τ being expressed as a number of sampling periods. Pg. 7 lines 30-34,

Claim 14 thereafter claims that a series of delay sub-lines, which originate from the delay line, are directly joined to a plurality of multiplexers for parallel recombination in a coherent manner. As stated on page 11, lines 11-13, all the various samples received of the received input signals are then recombined in a coherent manner to recover the common information. Pg. 11, lines 11-13. The parallel recombination of the samples is discussed on at least page 11, beginning at line 20.

Claim 14 further describes now two series of samples can be read in parallel with separate memory areas being regrouped into a first group and a second group. As described on page 20, beginning at line 25, the memory areas can be regrouped as GROUPA and GROUPB as shown in the Table of Fig. 12. The first group GROUPA regroups a current series C_BANK and a next series NEXT_BANK corresponding both of them to the second series of delay sub-lines BANK1. The second group GROUPEB regroups a current series C_BANK and a next series NEXT_BANK wherein both of them corresponding to the second series of delay sub-lines BANK1.

Consequently, instead of choosing in a first period the series of memory areas in which current chip is situated, then selecting the proper memory areas of the current useful samples as a function of the value of the position factor, the proper memory areas are selected as a function of the value of the position factor in each of the two groups after which the series of memory areas is selected in which the current chip is situated. See Pg. 20 line 35 to page 21, line 2.

The aforementioned description of the claimed subject matter references page and line number of the specification as originally filed. The filing of February 16, 2005 was based on a French PCT filing with a corresponding WO translation. This application, WO2004/019510, is the basis for the cited text above. Many examples and illustrations of the claimed invention are present in the specification and accompanying figures which can be used in combination with the above description to more fully appreciate details of the present invention.

VI. Grounds of Rejection to be Reviewed on Appeal

Claims 1-10, 12 and 13 stand rejected under 35 USC § 103(a) as being unpatentable over U.S Patent Application Publication No. 2002/0037027 by Medlock ("Medlock") in view of Appellant Admitted Prior Art (AAPA). Claim 11 stands rejected over Medlock and AAPA, in further view of U.S. Patent 6,788,731 by Kim ("Kim"). Claim 14 stands rejected over Medlock in view AAPA and in further view of Kim.

The grounds of rejection of claims 1, 6, 12, 13 and 14 is to be reviewed on this Appeal.

VII. Argument

A. CLAIMS 1, 12, 13, AND 14 ARE PATENTABLE AS THE CITED PRIOR ART FAILS TO TEACH OR SUGGEST THE GENERATION OF READ ADDRESSES IN DELAY SUB-LINES BASED ON DIFFERENCES BETWEEN THE WRITE ADDRESS AND THE DELAY

Claim 1 states, inter alia, a "control means configured to generate ... read and write addresses of the samples in the delay sub-lines from the series of samples of the input signal, so that a read address is equal to a difference between the write address of the single sample in a delay sub-line of the input signal and a delay expressed as a number of sampling periods from the series of delays." Claims 12, 13 and 14 have similar renditions with respect to the same generation of the read address. This feature of the present invention is not present in Medlock nor has it been disclosed as AAPA. Accordingly, the prima facie case of obviousness is wanting for evidence showing that the prior art teaches or suggests each and every element of the claimed invention either explicitly or inherently.

1. Medlock fails to expressly teach generation of a read address as claimed by the present invention.

In the rejection leading to this review, Medlock is cited (paragraphs [0056, 0063]) for generating read and write addresses in delay sub-lines from a series of

samples of input signals, after the last sample as been received, so that the read address is equal to a difference between the write address of the single sample in the delay sub-line and the delay expressed as a number of sampling periods from the series of delays. However, a careful examination of the cited Figures (Figures 9 and 10) and the cited paragraphs provides no such teaching.

Paragraph 56 states:

> FIG. 7 illustrates an exemplary memory 304 in accordance with an embodiment of the invention. The memory 304 includes multiple registers 702a-702p. Each register 702 is divided into two halves: one half for storing In-Phase (I) data and another half for storing Quadrature (Q) data. Decimated samples from the decimation circuit 302 are sequentially written into the multiple registers 702 in a circular manner, one sample being stored in each register. Thus, when all the registers 702 have been initially written into, the next sample is written into the least recently written register and so forth. For example, if there are 16 registers and the samples are stored in numerical order starting with sample 0, then sample 16 is stored by overwriting sample 0, sample 17 is stored by overwriting sample 1, etc. as shown in FIG. 7. This way, the memory 304 contains the most recent samples from the decimation circuit 302. The number of registers shown in memory 304 of FIG. 7 is arbitrary and can be increased or decreased depending on system requirements. (emphasis added)

Paragraph 63 states:

> FIG. 10 illustrates another exemplary despreading circuit 600 coupled to the memory 304 as shown in FIG. 9 above. In FIG. 10, each memory block 902 in the memory 304 is further divided into segments 1002a-1002h. In an exemplary embodiment, the size of the segments 1002 is dependent on area minimization. For example, for a memory block of 256 word (or chip) size, a 16 or 32 word segment 1002 is a good performance trade-off. A person skilled in the art knows how to calculate a performance area trade-off and determine an optimum size for the segments 1002 based on the memory block size. Each memory segment 1002 is coupled to a separate bussing element 1004a-1004h via multiple signal lines 1006a-1006h. In general, each signal line 1006 carries an I and Q data pair onto the bussing element 1004. Each bussing element 1004 sequentially reads out data from its respective segment 1002. (emphasis added)

In KSR the court reaffirmed the *Graham* factors in the determination of obviousness under 35 U.S.C. § 103. *See KSR International Inc. v. Teleflex Inc.*, 127 S.Ct.1727 (2007). Specifically, the obviousness analysis is based on four underlying

factual inquiries, the well-known *Graham* factors: (1) the scope and content of the prior art; (2) the differences between the claims and the prior art; (3) the level of ordinary skill in the pertinent art; and (4) secondary considerations, if any, of nonobviousness. *Graham v. John Deere Co.*, 383 U.S. 1, 17-18 (1966); *Kegel Co., Inc. v. AMF Bowling, Inc.*, 127 F.3d 1420, 1430, 44 USPQ2d 1123, 1130 (Fed. Cir. 1997). The court in KSR did not reject the fact that the prior art reference (or references when combined) must teach or suggest all the claim limitations. *Id.* What a reference teaches is a question of fact. *In re Beattie*, 974 F.2d 1309, 1311 (Fed. Cir. 1992) (citing *Panduit Corp. v. Dennison Mfg. Co.*, 810 F.2d 1561, 1579 n.42, 1 USPQ2d 1593, 1606 n.42 (Fed. Cir. 1987)).

This teachings of the Supreme Court is reiterated in the MPEP §706.06(j) where this USPTO Board of Appeals and Interferences is quoted as stating, "To support the conclusion that the claimed invention is directed to obvious subject matter, either the references must expressly or impliedly suggest the claimed invention or the examiner must present a convincing line of reasoning as to why the artisan would have found the claimed invention to have been obvious in light of the teachings of the references." MPEP §706.06(j) quoting *Ex parte Clapp*, 227 USPQ 972, 973 (Bd. Pat. Ap. & Inter. 1985).

It is clear, therefore, that to establish prima facie obviousness of a claimed invention, all the claim limitations must be taught or suggested by the prior art. *In re Royka,* 490 F.2d 981, 180 USPQ 580 (CCPA 1974).

Claims 1, 12, 13 and 14 each require, in varying language, "generate ... read and write addresses of the samples in the delay sub-lines from the series of samples of the input signal, so that a read address is equal to a difference between the write address of the single sample in a delay sub-line of the input signal and a delay expressed as a number of sampling periods from the series of delays."

Medlock offers no such teaching or suggestion of address generation in which the read address is equal to the difference between the write address in a delay sub-line of the input signal and a delay expressed as a number of sampling periods from the series of delays.

The claims clearly state that a first element in determining the read address is first knowing the write address in a delay sub-line. Examining the teachings of paragraphs [0053] and [0063] of Medlock as well as the depictions shown in Figure 10, it is clear that Medlock employs a circular buffer as is asserted by the Examiner in his rejection. Medlock states that as inputs are received samples "are sequentially written into the multiple registers 702 in a circular manner, one sample being stored in each register" Medlock [0053] (emphasis added). And, in keeping with the teachings of a circular buffer, "Each bussing element 1004 sequentially reads out data from its respective segment 1002." Medlock [0063] (emphasis added)

Medlock does not teach or suggest the generation of a read address equal to a difference between the write address of the single sample in a delay sub-line of the input signal and a delay expressed as a number sampling periods from the series of delays. Medlock teaches a sequential loading of a circular buffer. While each sample does possess its own memory register, similar to what is claimed by the Appellant, it does not teach or suggest a write address of a delay sub-line possessing a single sample. This conclusion draws from the fact that there are no delay sub-lines in Medlock prior to memory storage. The memory segments referred to in Medlock (1002a-1000h in Figure 10) reference the multiple registers are loaded sequentially.

Recall that claim 1 states, among other things "... delay line is ... divided into a series of delay sub-lines, each sub-line being used to write only a single sample from the series of samples of said input signal, each of the delay sub-lines including a separate memory area to receive the single sample from the series of samples...." While the division of the delay line into sub-lines appears to be a trivial difference from that of Medlock when considering loading the samples into separate memory locations, the significance of the claimed approach becomes apparent when considering that it is the structure of multiple sub-lines that provides the means for determining a difference between the write address of the single sample in a delay sub-line of the input signal and a delay expressed as a number of sampling periods from the series of delays.

The Examiner argues that Medlock teaches an offset or difference between the read and write blocks since the reading and writing are performed in different blocks.

The Examiner then concludes that a time difference between two delay segments would be a sample period. Paragraph [0056] of Medlock teaches that register is divided into two halves wherein each half stores a sequential portion of a decimated sample. Paragraph [0073] (cited by the Examiner) also describes how the memory is divided into segments and each segment contains an I and Q data pair.

The Examiner concludes without supporting evidence, that there is an offset or difference between the read and write addresses. There is no explicit teaching of such a conclusion in Medlock. Moreover, the Examiner then takes that unsupported conclusion to further deduce that since the samples are placed in separate memory registers, the time difference between two delay segments would be a sample period. Again, such a teaching is not present in Medlock. And, even if such a conclusion did exist in Medlock, that is not what is claimed in the present invention.

The present invention claims a read address is equal to a difference between the write address of the single sample in a delay sub-line of the input signal and a delay expressed as a number of sampling periods from the series of delays. The Examiner relies on his own knowledge to reach the conclusion that Medlock teaches the present invention. As stated in MPEP 707.05(2) "When a rejection in an application is based on facts within the personal knowledge of an employee of the Office, the data shall be as specific as possible, and the reference must be supported, when called for by the Appellant, by the affidavit of such employee, and such affidavit shall be subject to contradiction or explanation by the affidavits of the Appellant and other persons." The Appellant refutes the Examiner's conclusion and seeks evidence from the Examiner in support of his supposition.

In effect, the Examiner, without stating so, relies on Official Notice that an offset exist and that a read address would be generated as claimed. The Appellant rejects the assertion that such a conclusion is well-known or is so common knowledge in the art that it is capable of instant and unquestionable demonstration as being well-known. See *In re Ahlert*, 424 F.2d 1088, 1091, 165 USPQ 418, 420 (CCPA 1970) see also *In re Knapp Monarch Co.*, 296 F.2d 230, 132 USPQ 6 (CCPA 1961)). Having asked for support of the conclusions reached in the present rejection, the Examiner has provided none. The Office has failed to meets its burden of proof.

That which is contained within the four corners of Medlock fails to teach or suggest at least this limitation for the claimed invention.

2. Medlock fails to impliedly teach or suggest generation of a read address as claimed by the present invention.

Medlock also fails to impliedly teach the generation of a read address so that the read address is equal to a difference between the write address of the single sample in a delay sub-line of the input signal and a delay expressed as a number of sampling periods from the series of delays.

The Appellant agrees with the Examiner and concedes that Medlock teaches a circular buffer. As stated in the Advisory Action, Medlock decimates received data by a certain factor, stores the data in a circular buffer, and then reads the data from memory as needed by the interpolation circuit. See Medlock paragraph [0065] and Advisory Action of January 28, 2010. Paragraphs [0072-0074] of Medlock discuss memory addressing but is void of any insinuation of generating read and write addresses so that the read address relates to the difference between the write addresses and the signal delay.

The conclusion reached by the rejection, that there is an offset between the read and write addresses to avoid collisions, does not teach, suggest or imply the stated limitation. Furthermore, the fact that Medlock appears to follow a different approach to generation of read and write addresses that would lead one of reasonable skill in the relevant art down a different path, apart from that claimed by the present invention.

Medlock teaches a system in which the "memory address ... is formed by dividing the sample address by the number of samples stored at each memory address." Medlock at [0073] fails to mention or imply in any way that the read address would be equal to a difference between the write address of the single sample in a delay sub-line of the input signal and a delay expressed as a number of sampling periods from a series of delays.

Just as Medlock fails to explicitly teach or suggest each and every limitation of the present invention, it also fails to imply the recited requirements. "To support the conclusion that the claimed invention is directed to obvious subject matter, either the references must expressly or impliedly suggest the claimed invention or the examiner must present a convincing line of reasoning as to why the artisan would have found the claimed invention to have been obvious in light of the teachings of the references." MPEP §706.06(j) quoting *Ex parte Clapp*, 227 USPQ 972, 973 (Bd. Pat. Ap. & Inter. 1985). Moreover, "[R]ejections on obviousness grounds cannot be sustained by mere conclusory statements; instead, there must be some articulated reasoning with some rational underpinning to support the legal conclusion of obviousness." (*In re Kahn*, 441 F. 3d 977, 988 (CA Fed. 2006) cited with approval in KSR) .

Medlock fails to expressly teach or impliedly suggest the claimed invention. The Examiner has offered no line of reasoning as to why an artisan of reasonable skill would have found the claimed invention obvious in light of the teachings. That is, the Examiner has offered no reason why, in light of the teaching of Medlock, an artisan of reasonable skill in the art would find the generation of a read address as claimed obvious. Instead, the Examiner forwards that "It would have been obvious to one having ordinary skill in the art at the time the invention was made to have the early, in-time, and late outputs, recombined to a plurality of demodulators in coherent manner so as to recover the initial input signal to its original form according to the delay." Final Office Action at pg. 5. The Examiner offers no reasoning with respect to the conclusion that one skilled in the art in light of Medlock would find the address generation scheme claimed by the present invention obvious.

The rejections of claims 1, 12, 13 and 14 each rely on Medlock to teach or suggest the generation of a read address so that the read address is equal to a difference between the write address of the single sample in a delay sub-line of the input signal and a delay expressed as a number of sampling periods from the series of delays. Medlock, however, fails to expressly or impliedly teach or suggest such a limitation and the Examiner has failed to present a convincing argument why one of reasonable skill in the art at the time the invention was made would find the limitation

obvious in light of Medlock. The remaining pieces of art, AAPA and Kim fail to resolve this deficiency.

The Appellant respectfully submits that the Examiner has failed to present a prima facie case of obviousness. Accordingly, the Appellant requests that the rejection be overturned placing the case in condition for allowance.

B. MEDLOCK FAILES TO TEACH OR SUGGEST THAT SAMPLES OF A SERIES OF SAMPLES ARE ACCESSIBLE IN PARALLEL IN THE WRITE MODE AS IS RECITED IN CLAIM 6

Claim 6 stands rejected as being obvious over Medlock in view of AAPA. Claim 6 characterizes the receiver of claim 1 in that the samples of a series of samples are accessible in parallel in the write mode or read mode in the delay sub-lines. The rejection of claim 1 implies that Medlock Fig. 10, parallel sub-lines 1004-1004h, teach this feature of the present invention. Figure 10 is described in paragraphs [0063-0064] of Medlock. There Medlock states, "In general, each signal line 1006 caries an I and Q data pair onto the bussing element 1004. Each bussing element sequentially reads out data from its respective segment 1002."

Assuming for arguments sake that each memory segment 1002 includes a single sample, it appears that the bussing elements 1004a-h couple each of the memory segments 1002a-h to a common bus 1010. Indeed, paragraph [0064] states that "Multiple dispreading circuits 600a-600b are connected to the memory segments 1002 via a bus 1010."

As pointed out by the Examiner, Medlock teaches a circular buffer. It is clear from the teachings of paragraph [0056] and [0063] that data is written to and read from the circular buffer sequentially. Indeed a circular buffer is well suited to a first in – first out type of buffer.

Claim 6 however, consistent with the teachings of claim 1, calls for the ability to access the samples, both in a write and read mode, in parallel. Medlock not only fails to teach or suggest such a limitation but indeed teaches away from the claimed

invention. Medlock teaches sequential writing and reading of the samples not that the samples are accessible in parallel in a write or read mode in the delay sub-lines.

Conclusion

In view of all of the above, claims 1, 12, 13, and 14 are believed to be allowable and the case in condition for allowance. As claims 2-11 depend from claim 1, they too are deemed allowable and in condition for allowance. Appellant respectfully requests that the Examiner's rejections based on 35 U.S.C. § 103(a) be reversed for the pending claims.

Respectfully submitted,

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VIII. CLAIMS APPENDIX

1. A receiver for receiving an input signal comprising a series of samples, said receiver comprising one delay line, characterized in that the delay line is configured to delay said input signal by a series of delays and is divided into a series of delay sub-lines, each sub-line being used to write only a single sample from the series of samples of said input signal, each of the delay sub-lines including a separate memory area to receive the single sample from the series of samples, and further comprising control means configured to generate, after a last sample of the series of samples is received, read and write addresses of the samples in the delay sub-lines from the series of samples of the input signal, so that a read address is equal to a difference between the write address of the single sample in a delay sub-line of the input signal and a delay expressed as a number of sampling periods from the series of delays, and wherein the delay sub-lines are directly joined to a plurality of multiplexers for providing early, in-time, and late outputs, and thereafter to a plurality of demodulators for parallel recombination in a coherent manner to find common information according to the delay.

2. A receiver as claimed in claim 1, characterized in that the delay line comprises a single series of delay sub-lines.

3. A receiver as claimed in claim 1, characterized in that the delay line comprises various series of delay sub-lines.

4. A receiver as claimed in claim 1, characterized in that a delay sub-line is accessible with a frequency twice as fast as the samples of an input signal received by the receiver.

5. A receiver as claimed in claim 1, characterized in that one memory area is associated to one delay sub-line.

6. A receiver as claimed in claim 1, characterized in that the samples of a series of samples are accessible in parallel in the write mode or read mode in the delay sub-lines.

7. A receiver as claimed in claim 1, characterized in that the read addresses of the samples of a series of samples are situated at addresses immediately adjacent or equal to one another.

8. A receiver as claimed in claim 3, characterized in that two series of samples are read in parallel.

9. A receiver as claimed in the preceding claim 8, characterized in that the delay line comprises selection means of a series of delay sub-lines to which belongs one of the two series of samples read as a function of the delay.

10. A receiver as claimed in claim 1, characterized in that the delay line comprises a position factor indicating the position of a reference sample from a series of samples of an input signal in the series of delay sub-lines to which it belongs.

11. A receiver as claimed in the preceding claim 8, characterized in that the memory areas are regrouped into a first and a second group, the first group regrouping a current series of current areas and a next series of areas which can each correspond to the first series of delay sub-lines and the second group regrouping the current series of areas and the next series of areas which can each correspond to the second series of the delay sub-lines, so that the memory areas for a series of samples read are identical for each equal position factor value.

12. A delay line for delaying an input signal, said input signal comprising a series of samples, characterized in that the delay line is configured to delay said input signal by a series of delays and is divided into a series of delay sub-lines each sub-line being used to write only a single sample from the series of samples of said input signal, each of the delay sub-lines including a separate memory area to receive the single sample from the series of samples, and in that the delay line comprises control means configured to generate, after a last sample of the series of samples is received, read and write addresses of the samples in the delay sub-lines from the series of samples of the input signal, so that a read address is equal to a difference between the write address of the single sample in a delay sub-line of the input signal and a delay expressed as a number of sampling periods of the series of delays, and wherein the

delay sub-lines are directly joined to a plurality of multiplexers for providing early, in-time, and late outputs and therefore to a plurality of demodulators for parallel recombination in a coherent manner to find common information according to the delay.

13. A method of delaying an input signal by means of a delay line, said input signal comprising a series of samples, characterized in that it comprises the steps of:

dividing the delay line into a series of delay sub-lines each sub-line configured to receive a single sample from the series of samples of the input signal, each of the delay sub-lines including a separate memory area to receive the single sample, said delay line being configured to delay said input signal by a series of delays,

generating, after the single sample of the series of samples is received, read and write addresses of the samples in the delay sub-lines from the series of samples of the input signal, so that a read address is equal to a difference between the write address of the single sample in a delay sub-line of the input signal and a delay expressed as a number of sampling periods of the series of delays, and

directly joining the delay sub-lines to a plurality of multiplexers for providing early, in-time, and late outputs, and thereafter to a plurality of demodulators for parallel recombination in a coherent manner to find common information according to the delay.

14. A receiver for receiving an input signal comprising a series of samples, said receiver comprising one delay line, characterized in that the delay line is configured to delay said input signal by a series of delays and is divided into a series of delay sub-lines each sub-line being used to write only a single sample from the series of samples of said input signal, each of the delay sub-lines including a separate memory area to receive the single sample from the series of samples, and further comprises control means configured to generate, after the single sample of the series of samples is received, read and write addresses of the samples in the delay sub-lines from the series of samples of the input signal, so that a read address is equal to a difference between the write address of the single sample in a delay sub-line of the input signal and a delay expressed as a number of sampling periods from the series of delays, wherein the delay line comprises various series of delay sub-lines joined directly to a

plurality of multiplexers for parallel recombination in a coherent manner, two series of samples are read in parallel, and the separate memory areas are regrouped into a first and a second group, the first group regrouping a current series of current areas and a next series of areas which can each correspond to the first series of delay sub-lines and the second group regrouping the current series of areas and the next series of areas which can each correspond to the second series of the delay sub-lines, so that the separate memory areas for a series of samples read are identical for each equal position factor value.

IX. EVIDENCE APPENDIX

No copies of evidence are required with this Appeal Brief. Appellant has not relied upon any evidence submitted under 37 C.F.R. §§ 1.130, 1.131, or 1.132.

X. RELATED PROCEEDINGS APPENDIX

There are no copies of decisions rendered by a court or the Board to provide with this Appeal as there are no related proceedings.